PowerXL

DA1

Firmware Release Note

Powering Business Worldwide

Eaton Addressees

Eaton.com/contacts
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Original Release Note is the English version of this document.

All non-English language versions of this document are translations of the original Release note.

Content

1 V2.40 Change Notification – 01.02.2019

Existing Version 2.00 (DA1)
New Version 2.40 (DA1)

Management Summary

We updated the firmware of DA1 for your convenience. The use of existing parameter sets can generally be continued. The following updates will improve handling and functionality of the drive.

1. Functionality

1.1. Fix 2nd analog input 20…4mA option not working issue

In all previous release, the 20…4mA option in P2-33 (option 6 and 7) doesn't work for the 2nd analog input (unless analog input 1 is also set to 20...4mA mode). This issue is now fixed in this new software release.

1.2. Updated internal comms protocol with one byte checksum (4-bits)

In order to enhance the data transfer integrity under noisy application environment, an extra byte has been added into drive internal communication protocol for extra checking purpose. This will reduce the chance of error data and make sure correct information to be received between two processors in the drive. Only 4 bits of error checking is used due to compatibility and performance limitation.

1.3. Parameter P4-04 minimum limit increased

The minimum limit of P4-04 in now increased to 0.010.

1.4. P4-12 thermal overload retention default value changed

Default value of P4-12 has been changed from 0 to 1, so the thermal overload retention function is enabled by default.

1.5. 4..20mA signal loss trip now has a delay time of 500ms

There will be 500ms delay/filter time for detecting signal loss condition if any analog input is configured as 4..20mA input
This is used to filter out large noise signal on the analog input line to avoid false operation. The delay/filter in previous software is 24ms.

1.6. New PLC function block: flip-flop

New PLC function block for flip-flop action support has been added in this new software release.

1.7. Add new PLC function block “Trip Request”

A new PLC function block “Trip request” has been added into this release. This new function block can be used to trip the drive within the user PLC program. Trigger input can be configured as edger or level. Two trip codes can be used for this function block “PLC-09” and “PLC-10”.

1.8. New LCD display support

New LCD display support has been added into this release (except the new function button).

1.9. New OLED/LCD production test pattern display support

Two test display pattern has been added into this software release for production OLED/LCD test support.

To enable pattern 1 (checker board), set value 0x0014 to parameter index (0, 0, 255).

To enable pattern 2 (inverse checker board), set value 0x0024 to parameter index (0, 0, 255).

1.10. Special parameter read function for production in order to read LCD board information

Optibus parameter index (0, 0, 254) can be used to read LCD/OLED display board information. Content in this parameter includes: Display version (16bit), Language index (8bit), 2nd stir fan speed (8bit) and display checksum (16bit).

1.11. LCD display on board upgrade support

On board LCD display upgrade function is added in this release. Optibus parameter index (0, 0, 255 bit 11) is used to enable upgrade process.

1.12. Two extra buttons support

The two extra buttons on the LCD display panels are now supported by the drive, result can be read\used by user PLC program.

1.13. Optibus communication protocol optimisation

Various area of operation has been optimized, including display message handling, multiple device parameter read/write handling, drive parameter list description name modification without downloading the complete parameter set, etc.
Add new display message index to: 0x15 USEr-r, 0x16 PArA-r, 0x17 PLC-r. And LED text PASS-t changes to PArA-t. dL-PLC changes to PLC-t

1.14. Group zero block transfer method added

Group zero block transfer function support has been added in this release.

1.15. Heat sink fan speed control support

Support for new IP20 S6A/B PWM fan speed control has been added into this release. Fan will run at 30% (≤45˚C) to 100% (≥80˚C) of maximum speed based on heatsink temperature reading.

1.16. PID output limit regulation updated

An updated PID output limit control method has been implemented in this release:
When PID output is large than the maximum limit defined by P3-07, the output will be limited at this max level. The Integral loop output will not be limited until the PID error changes direction (from positive to negative).
When PID output is lower than the minimum limit defined by P3-08, the output will be limited at this min level. The integral loop output will not be limited until the PID error changes direction (from negative to positive).
Please note that when P3-09 set to 3, the PID output limit defined by P3-07 and P3-08 will take action before adding the analog input 1 as offset adjustment, so the final output of the PID loop could vary between 0% and 100% under such condition.

1.17. Add “O-I”, “h O-I”, “b O-I” and “I.t-trp” reset delay control

A progression reset delay time has been added for “O-I”, “h O-I”, “b O-I” and “I.t-trp”trip reset. The delay time will be 4s -> 8s -> 16s -> 32s -> 64s (maximum). The trip reset delay and trip accumulation time works as follows:
If drive trips O-I/h O-I for the first time, then it will take minimum 4s before trip can be reset. After reset, the trip accumulator will start, if dive trips again within next 4s, then the new reset delay time will be 8s. Once the trip being reset after 8s, the trip accumulator timer will start again. Within next 8s if trip happens again, the new trip reset delay will be increased to 16s. If trip happens after the next 8s but within next 16s the new trip reset delay will be keep at 8s. If the trip happens after next 16s, then new trip reset delay will be reduced to 4s.
This principle works up to 32s, if trip reset delay reach 64s, then after reset, it will need at least 64s for next trip reset delay to be reduced to 32s, as the maximum trip reset time is limited to 64s.
Please note that if ‘Fire’ mode is active, then the maximum delay time for reset will be 4s. However the trip accumulator time will be still running in background even in fire mode. So after fire mode being cleared, drive may need 4s/8s/16s/32s/64s to reset further O-I/h O-I trip as normal depends on how many and how frequent the O-I/h O-I trip happened previously.

1.18. Mains loss threshold level modified

For 400V drives, mains input loss threshold voltage level has been increased from 200V(AC) to 295V(AC).
For 230V drives, mains input loss threshold voltage level has been increased from 120V(AC) to 155V(AC).

1.19. Remove L1, L2 and L3 filter during mains loss condition

The internal filter for input voltage measurement value in P0-74, P0-75 and P0-76 will be disabled when drive is in Mains supply loss condition.

1.20. Overload condition changed

Faster integration rate (16x) transition only occurs at 150% of drive rated current instead of 150% of P1-08.

This limit also applies to PM or BLDC mode 200% over load condition (P4-07 >=200% and P4-01>=3 and <=5)

1.21. Low speed overload control

The overload integration at low speed (below 10% of P1-09) will be 5% faster than normal rate due to new UL requirement.

For example, at 150% overload for AC induction motor, the overload time will be 60s if motor output speed is large than 10% of rated speed. Otherwise it will be 57s if speed is less than 10% of rated speed.

1.22. Motor control enhancements

The new motor control library 167 has been used in the new software release (163 in the existing firmware release) with the following enhancements:

1.22.1. PI speed controller's integral time constant limited internally to 10ms

1.22.2. New DC current injection algorithm replaces previous DC voltage injection one.

Parameter P6-18 sets the % of drive rated current to be injected for the time specified in P6-12. This algorithm is active in VF, Smart-V and Vector mode of operation.

1.22.3. Improved spin start solution in encoder (Vector) and encoder-less (Vector and Smart-V) mode.

1.22.4. Improved generator/braking mode of operation

Work has been carried out on the existing rotor flux observer (RFO) to improve its behaviour during braking/generator mode operation.

1.22.5. Energy saving algorithm is always enabled for BLDC motors.

1.22.6. Speed error protection added in encoder-less vector when in hoist mode operation.

In previous versions the speed error protection was only active in encoder mode of operation. Now this protection has been enabled in encoder-less mode too, but only when in hoist mode.

1.22.7. Torque timeout protection added in V/F mode of operation.

1.22.8. Motor-tune parameters are now initialized to group 7 parameters before carrying out the auto-tuning.

This is done to avoid the situation where the auto-tune algorithm is interrupted by an external fault. In previous versions the group 7 was reset to zero, whereas with this change the drive will show the existing group 7.

1.22.9. Fixed O-I trip problem reported in stone cutter application.

1.22.10. Fixed O-I trip problem while trying to apply dc braking current to a motor running above base speed (100Hz)

1.22.11. Improved synchronous motor control to work with new generation of IE5 motors.

1.22.12. Anti-resonance FIR filter added to motor current in order to reduce chances of O-I trip when working with output filters. This filter was added previously on ECO v2.30 firmware and it has improved the drive's robustness against O-I trip, especially in smart vector mode of operation.

2 V2.50 Change Notification - 01.05.2023

Existing Version 2.40 (DA1)
New Version 2.50 (DA1)

This document details all of the changes which have been made between the Existing and New drive firmware versions indicated above.

1. **Power up sequence handling optimization**
   In certain application where multiple drives are connected together via RJ45 communication cable and are powered up with slightly time difference, e.g. different reaction time of input contactor etc. Certain drive in the network may show “Faulty” message which can only be reset after power cycle.

   In this new release, the power up checking sequence has been optimized to cope with this delay issue.

2. **P6-29 adds new option 3 and 4**
   Two new options have been added to P6-29:

   3: Reset to factory default

   4: Reset to user default

   Please note that if there is no user default settings saved and option 4 is selected, then drive will do factory default instead.

   New option 3 and 4 won’t work via parameter list download (e.g. Comstick transfer etc). Value will be ignored and reset to 0.

   This new option require new TFT/OLED software support (including keypad).

3. **Add CANopen heartbeat consumer function support**
   Support for CANopen object 0x1016 (sub index 0 and 1 only) has been added in this release

   We only support consuming heart beat from one CANopen node. The time out action is defined by P5-06.

   This function is disabled by default.

4. **Add support for new IP66 drive (Small drive control board)**
   Support for new IP66 drive integrated pot and switches function has been added into this release.

Production setup:

A new calibration parameter C-16 has been added into this release. Currently it has the value range from 0 to 3.

Bit 0 = Pot enable control, Bit 1 = Switches enable control

C-16 = 0: No pot and no switch (default status – IP20)

C-16 = 1: With pot and no switch

C-16 = 2: No pot and with switches

C-16 = 3: With pot and with switches

This calibration parameter will be setup during production calibration procedure. Service procedure should also take care of this change

For integrated pot function:

If integrated pot is enabled by setting C-16 bit 0 to 1 (e.g. C-16 = 1 or 3), then there will be a new option 8 in P2-30 (analog input 1 format) as “In-Pot”.

This new option 8 will be set as default value of P2-30 for new IP66 drive with integrated pot fitted (C-16 bit 0 is set). In this case, drive analog input 1 value will come from the integrated pot, main analog input via terminal input 6 will have no effect and the input will be configured as voltage input mode. Analog input offset P2-32 and scaling P2-31 parameters will work as normal on the integrated pot as well.

To disable the integrated pot function, user needs to manually set P2-30 to any other value range from 0 to 7.

The signal converted result of drive integrated pot is 12 bits (0 ~ 4096), however the physical resolution of the pot is 10 bits only (result will be digitally scaled up). The integrated pot analog convert value will be updated once every 12.8ms.

During parameter transfer (via Comstick or drivesConnect), if parameter list is transferred from a new IP66 drive to a IP20 drive with P2-30 set to 8, this parameter will be reset to 0 automatically if the target drive has software version v2.50 or later. Older version drive will configure analog input as current input mode. So care must be taken under such condition.

New version of drivesconnect will show option 8 as “Integrated Pot (IP66 only)” for both IP20 drive and IP66 drive.

For integrated switches function:

The integrated switches will work in parallel with drive terminal 2 (T2) and terminal 3 (T3) as digital input 1 and digital input 2. By default, the integrated switches are enabled (“Lc-OFF”) if C-12 bit 1 is set (e.g. C-16 = 2 or 3).

To disabled/enable the integrated switches function, user needs to do the following step:

1) Set correct value in P1-14 to enable advanced parameter access.

2) Go to “P0-xx” and make sure drive is in stop condition (not running, not tripped).

3) Press and hold “STOP” button for about 1s, drive will show “Lc-OFF”, “Lc-On” or “Altern” message. TFT display will show “IP66 switch setup”

4) Use “UP” or “DOWN” key to select the options:
“Lc-OFF” means integrated switches are enabled. (>> for Digital input 1, << for digital input 1 and 2)

“Lc-On” means the switches are locked/disabled.

“Altern” means alternative switch configuration function (>> for Digital input 1, << for digital input 2)

5) Press “STOP” button again to exit.

Please note that this access method is only available for the new IP66 drive with integrated switches fitted (C-16 bit 1 must be set to 1).

The integrated switches function setup can be copied from drive to drive by using new version of Comstick (v2.00 or later), older version Comstick will not transfer this switches setting.

Currently, PC software DrivesConnect doesn’t support this setting (drive parameter index 255) to be setup/transferred via parameter download.

5. **S2 S3 LV drive default switching frequency changed to 8kHz**
Default switching frequency in P2-24 for low voltage size 2 and size 3 drive has been reduced from 16kHz to 8kHz

6. **V/F curve control updated**
Re-enable Ud function and set to boost voltage level.

Uq now range from 0 instead of boost voltage level up to rated voltage level.

7. **Add support to new Size 3 and Size 4 LV single phase input drive**
This release adds support for the new S3 230V single phase input 4.0kW(5.0HP) drive, S4 230V single phase input 5.5kW(7.5HP) and 7.5kW(10HP) drives.

8. Motor control enhancements

The new motor control library 172 has been used in the new software release (167 in the existing firmware release) with the following enhancements:

a) Improved current control regulation during start-up of low impedance PM motors

While commissioning low impedance PM motors we have experienced O-I and hO-I trips following a start command. Hence the current regulation during mag time period has been modified to remove these errors.

b) New Autotuning algorithm

In order to support IP66 film capacitor drives, a new 'streamlined' autotuning algorithm had to be developed in order to make space for the new motor control software. This new algorithm has been heavily tested for more than 1yrs and results show no divergence against existing autotuting algorithm.

c) Improved full vector solution for IP20 and I66 drives.

In order to support IP66 drives(10% film cap) the existing motor control solution had to be modified to cope with both IP20 and IP66 drives. IP20 drives have been tested to check that the changes made to support IP66 do not have a negative effect on existing electrolytic capacitor drives. One area that has been modified is the flux controller in order to keep motor flux as high as possible when operating with 10% film caps. drives.

d) Vdc bus voltage control protection

When the Dc bus voltage is pumped up (ie. regen), our voltage level protection algorithm accelerates the motor in order to reduce the energy in the DC bus. In order to prevent dangerous over speeds, this protection is now disabled when the rotor speed is higher than 120% P1-01, or 120% P1-09, whichever is the highest, to allow for the Vdc over-volts trip to occur.
All 600V drive over voltage ramp control is disabled.

e) Improved spin start algorithm.

The spin start has been modified so now it takes less time (33% less time) to build up the flux in the motor in vector mode.

f) Low pass filter added on boost voltage (P1-11)

During tests it was found that there was a chance to damage the power stage IGBT output in V/f mode of operation by setting a high boost voltage value (P1-11). An internal low pass filter (LPF) has been added to this boost voltage, which limits the rate at which this voltage is applied to the motor, which also limits the rate of the current injected into the motor.

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Eaton addresses worldwide:
Eaton.com/contacts

Eaton Industries GmbH
Hein-Moeller-Str. 7- 11
D-53115 Bonn/Germany

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